Amendments to the Claims:

Claims 1-14 are pending. Please amend claims 1, 5, and 8 as follows. This listing of claims will replace all prior listings of claims in the application.

Listing Of Claims:

Claim 1 (currently amended): An area array semiconductor device comprising:

a circuit wiring substrate having a top face with a circuit wiring;

a semiconductor chip having a top face and a bottom face, the bottom face being mounted on the circuit wiring substrate and ~~the top or bottom~~ at least the top face is electrically connected with the circuit wiring; and

a sealing layer composed of a sealing resin positioned on the entire top face of the semiconductor chip and a portion of the top face of the wiring substrate;

wherein a thickness of the sealing layer on the top face of the semiconductor is smaller than a thickness of the sealing layer on the portion of the top face of the wiring substrate; and

wherein the sealing layer is formed such that a periphery of the sealing layer has an angle of 30° to 60° with respect to a corresponding side of the circuit wiring substrate.

Claim 2 (original): An area array semiconductor device according to claim 1, wherein the semiconductor chip is mounted on the circuit wiring substrate such that the semiconductor chip has substantially the same angle as an angle which the side of the sealing layer composed of the sealing resin has with respect to the side of the circuit wiring substrate.

Claim 3 (original): An electronic circuit board comprising:

a printed wiring board as a mother board; and

an area array semiconductor device according to claim 1,

wherein the area array semiconductor device is soldered to the printed wiring board as the mother board.

Claim 4 (original): An electronic circuit board according to claim 3, wherein the area array semiconductor device is soldered to the printed wiring board with a lead-free solder.

Claim 5 (currently amended): An area array semiconductor device comprising:

an insulating interposer having a circuit;

an integrated circuit chip having a top surface and a bottom surface, wherein the bottom surface of the chip is mounted on a top surface of the insulating interposer and ~~the top or bottom~~ at least the top surface of the chip is electrically connected to the circuit of the interposer, the chip having a plurality of sides, each of the sides being at an angle of 30° to 60° with respect to a corresponding side of the interposer;

a resin provided on the entire top surface of the chip and a portion of the top surface of the insulating interposer,

wherein a thickness of the resin on the top surface of the chip is smaller than a thickness of the resin on the portion of the top surface of the insulating interposer; and

wherein the resin has an outer boundary of a plurality of sides angled at the same angle with respect to the interposer as the integrated circuit chip.

Claim 6 (previously presented): An area array semiconductor device according to claim 5, wherein the angle between the sides of the integrated circuit chip and the interposer is 45°.

Claim 7 (previously presented): An area array semiconductor device according to claim 5, wherein a periphery of the resin does not extend to a periphery of the interposer.

Claim 8 (currently amended): An electronic circuit board comprising:

a printed wiring board;

an insulating interposer defining an upper and a lower surface, the interposer having a plurality of connecting lands and a plurality of solder balls providing electrical connection to the wiring board; the interposer also having a circuit;

an integrated circuit chip having an upper surface and a lower surface, wherein the lower surface of the chip is in contact with the upper surface of the interposer and ~~the upper or lower~~ at least the upper surface is electrically connected to the circuit of the interposer, and the chip has a plurality of sides, each of the sides being at an angle of 30° to 60° with respect to a corresponding side of the interposer;

a protective material provided on the entire upper surface of the chip and a portion of the upper surface of the insulating interposer, which is adapted, in conjunction with the insulating interposer, to provide protection from contamination and moisture in the atmosphere, and the material having an outer boundary of a plurality of sides angled at the same angle with respect to the interposer as the integrated circuit chip,

wherein a thickness of the protective material on the top face of the chip is smaller than a thickness of the resin on the portion of the top surface of the insulating interposer.

Claim 9 (previously presented): An electronic circuit board according to claim 8, wherein the solder balls are made from a lead-free solder having a melting point greater than 183°C.

Claim 10 (previously presented): An electronic circuit board according to claim 9, wherein the solder balls have a melting point of 220°C.

Claim 11 (previously presented): An electronic circuit board according to claim 8, wherein the material also provides thermal insulation for the chip.

Claim 12 (previously presented): An electronic circuit board according to claim 8, wherein the material is applied to the upper surface of the interposer and entirely encapsulates the chip between the material and the interposer.

Claim 13 (previously presented): An electronic circuit board according to claim 8, wherein the material is a moldable material.

Claim 14 (previously presented): An area array semiconductor device according to claim 1, wherein the semiconductor chip is mounted on the circuit wiring substrate such that a side of the semiconductor chip is arranged parallel to the side of the circuit wiring substrate.